What is claimed is:

1. A method comprising:

detecting a condition in a processor;

calculating adjustment values at stages within a pipeline of the processor; and

updating a register with one of the adjustment values when an instruction associated with the condition is terminated within the pipeline.

2. The method of claim 1, wherein calculating the adjustment values comprises:

incrementing the adjustment values when the condition is detected; and

decrementing the adjustment values when the instruction leaves the stages.

3. The method of claim 1, wherein detecting a condition comprises detecting an access to a specified memory location.

4. The method of claim 1, wherein detecting the condition comprises detecting an instruction within a hardware loop.

Cont A7

5. The method of claim 4, wherein detecting the instruction within the hardware loop comprises detecting a bottom match.

6. The method of claim 1, wherein detecting a condition comprises detecting a watch point.

7. The method of claim 1, wherein updating the register with one of the adjustment values comprises adjusting the register by an amount determined by a counter residing in the stage where the termination occurred.

8. The method of claim 1, wherein updating the register comprises updating a speculative register.

9. A apparatus comprising:

a first register;

a second register; and

a set of counters to monitor a difference between the first register and the second register.

10. The apparatus as in claim 9, wherein the first register is a speculative register and the second register is an architectural register.

11. The apparatus as in claim 10, wherein the first register is a speculative count register and the second register is an architectural count register.

12. The apparatus as in claim 9, wherein the first register, second register and set of counters reside in a multi-stage pipeline controlled by a control unit, and the set of counters include counters maintained at a stage where the first register resides and at stages after the stage where the first register resides.

13. The apparatus as in claim 12, wherein the set of counters consist of counters residing at stages before an n^{th} stage of a pipeline, and wherein n defines a point at which allowing instructions to flow through the pipeline takes an amount of time less than or equal to a branch penalty.

14. The apparatus as in claim 12, wherein following a termination of an instruction in the pipeline, the control unit is adapted to adjust the first register by an amount determined by a particular counter maintained in a stage where the termination occurred.

A7

15. The apparatus as in claim 12, wherein the control unit is adapted to:

increment the counters when the first register is adjusted because of a detected condition; and

decrement a respective counter when the instruction leaves a respective stage associated with the respective counter.

16. A system comprising:

a static random access memory device;

a first register;

a second register;

a set of counters; and

a processor coupled to the static random access memory device, wherein the processor includes an execution pipeline and a control unit adapted to:

increment the counters when the first register is adjusted because of a detected condition; and

decrement a respective counter when the instruction leaves a respective stage of the pipeline associated with the respective counter.

17. The system of claim 16, wherein following a termination of the pipeline, the control unit is adapted to adjust the first register.

18. The system of claim 17, wherein control unit is adapted to adjust the first register by an amount determined by one of the set of counters.

19. The system of claim 18, wherein the one of the set of counters is a particular counter residing in a stage of the pipeline where the termination occurred.

20. The system of claim 17, wherein the control unit is adapted to drain unaborted instructions and write the first register with the data in the second register, if the termination occurs in a stage of the pipeline after an n^{th} stage.